REMARKS

Claims 1-10, 12-15 and 24-27 were pending in the Application. Claim 1 is an independent claim and claims 2-9 depend therefrom. Claim 10 is an independent claim and claim 12 depends therefrom. Claim 13 is an independent claim and claims 14-15 depend therefrom. Claim 24 is an independent claim. Claims 26 is an independent claim and claim 27 depends therefrom. Claims 11, 16-23 and 28-40 were previously canceled. Claims 10, 12-13, 15, 24 and 26 are currently amended. Claim 25 is currently canceled. Applicant respectfully requests reconsideration of the application in light of the above amendments and the following remarks.

Rejections Under 35 U.S.C. §112, First Paragraph (Claims 1-9, 25 and 27)

In points 4-6 on pages 2-3 of the Office Action, claims 1-9, 24 and 27 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. (Office Action, Point 4, Page 2). Specifically, the Office Action alleged that the "Applicant's Specification does not contain support for the limitations of 'wherein the first state comprises at least a portion of a memory address of the first memory block, irrespective of a position of the first logic circuit' (claim 1) and 'wherein the first state comprises at least a portion of a memory address of the block of memory segments irrespective of a position of the first logic circuit' (claim 25) since in Applicant's Specification, the addresses of memory blocks are related to the position of the identified available blocks within logic circuits indicating block availability." (Office Action, Point 5, Page 3).

However, the Applicant's Specification explicitly states the following:

> The address-determining step 1040 determines an address of the available memory segment corresponding to the previously-identified segment flag and optionally, the previously-identified block flag. **The address-determining step 1040 may be accomplished in a variety of ways**. For example, **various**

> **information may be contained in the segment or block flags that the step 1040 may utilize to calculate the segment address. Alternatively, for example, the step 1040 may convert the position of the identified segment flag** in the set of segment flags to the address of the memory segment.

(Applicant's Specification, Paragraph [96], Lines 3-9 (emphasis added)). Thus, as clearly shown above, the Applicant's Specification unmistakably sets forth a variety of alternate embodiments for determining a segment address, including calculating the segment address irrespective of a position of the first logic circuit (i.e., using information comprised in the first state).

The Applicant notes that the Office Action alleges that the cited section of the Applicant's Specification does not support the Applicant's claim limitations. However, as one of ordinary skill in the art would readily be able to ascertain, the Applicant's claim limitations (i.e., "irrespective of a position of the first logic circuit") are clearly supported by Applicant's explicit teachings of using information contained in the segment or block fags to calculate the segment address instead of (i.e., alternatively) converting the position of the identified segment flag and/or the identified block flag. Thus, the Office Action's assertion that at least the cited section of the Applicant's Specification fails to support the Applicant's claim limitations amounts to clear error and cannot be maintained.

With regard to point 6 of the Office Action, the Applicant respectfully notes that claim 27 does not depend from a rejected base claim (i.e., a claim containing the "irrespective of a position of the first logic circuit" limitation). Instead, claim 27 depends from claim 26, which previously depended from claim 24. Thus, the Applicant respectfully notes that the rejection of claims 27 is inappropriate.

For at least the reasons set forth above, the Applicant respectfully requests that the rejections of claims 1-9, 25 and 27 under 35 U.S.C. §112, first paragraph, be withdrawn.

Rejections Under 35 U.S.C. §103(a) – Goldberg and Lehman (Claims 10, 12-15 and 26-27)

In points 21-26 on pages 14-20 of the Office Action, independent claims 10, 13 and 26, and dependent claims 12, 14-15 and 27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Goldberg (U.S. Patent No. 6,874,062) in view of Lehman (U.S. Patent No. 6,658,437). The Applicant respectfully traverses the above-mentioned rejections for at least the following reasons.

In order for a *prima facie* case of obviousness to be established, the Manual of Patent Examining Procedure, Rev. 6, Sep. 2007 ("MPEP") states the following:

> The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Federal Circuit has stated that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."

See the MPEP at § 2142, citing *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006), and *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d at 1396 (quoting Federal Circuit statement with approval). Further, MPEP § 2143.01 states that "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the results would have been predictable to one of ordinary skill in the art" (citing *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (2007)). Additionally, if a *prima facie* case of obviousness is not established, the Applicant is under no obligation to submit evidence of nonobviousness:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

See MPEP at § 2142.

Regarding claim 10, Applicant respectfully submits that the proposed combination of

references fails to teach, suggest, or disclose at least, for example, "wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block, said number of available memory segments corresponding to at least the first state of the second logic circuit and the first state of the third logic circuit" and "wherein the first state of the first logic circuit is separate from the first state of the second logic circuit and the first state of the third logic circuit," as set forth in Applicant's independent claim 10.

The Applicant appreciates the Examiner's acknowledgement that Goldberg fails to teach "wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block, said number of available memory segments corresponding to at least the first state of the second logic circuit and the first state of the third logic circuit," as recited in Applicant's independent claim 10. (Office Action, Page 16, Lines 7-8). However, the Office Action alleges that Lehman's disclosure of a string teaches the Applicant's claim limitations. (Office Action, Page 16, Lines 9-18). The Applicant notes that the Office Action mischaracterizes Lehman and the Applicant's claims. Specifically, even if Lehman's bit string could be considered a first state of a first logic circuit comprising a number of available memory segments in a first memory block (which is clearly not taught by Lehman), Lehman still fails to disclose "said number of available memory segments corresponding to at least the first state of the second logic circuit and the first state of the third logic circuit," as recited in Applicant's independent claim 10. In other words, Lehman's bit map corresponds to available memory segments, not first states of second and third logic circuits. Thus, Lehman fails to remedy the deficiencies of Goldberg in that the combination of references clearly fail to teach "wherein **the first state of the first logic circuit comprises a number of available memory segments** in the first memory block, **said number of available memory segments corresponding to at least the first state of the second logic circuit and the first state of the third logic circuit**," as recited in Applicant's independent claim 10.

The Applicant notes that although the Office Action explicitly acknowledges Goldberg's failure to teach the Applicant's claim limitations (Office Action, Page 16, Lines 7-8), the Response to Arguments section of the Office Action inconsistently states that "Applicant should note, that

every bit of Bitmap 1 comprises a number of available memory sections/segments in LLB." (Office Action, Page 22, Lines 11-14). The Applicant notes that the Office Action mischaracterizes Goldberg. Specifically, Goldberg discloses setting a bit to either indicate that segments are available or no segments are available. (Goldberg, Figures 5-6, Column 9, Line 26 – Column 10, Line 50). For example, Goldberg's bit 502 in Bitmap 1 500 merely indicates that memory segments are available in LLB section 402 of LLB 400. (Goldberg, Figure 5, Column 9, Lines 32-39). However, nowhere in Goldberg is there any teaching that Goldberg's bit 502 in Bitmap 1 500 comprises a number of available memory segments (i.e., 10 memory segments) that are available in LLB section 402 of LLB 400 as alleged in the Office Action. Thus, as was previously acknowledged in the Office Action (Office Action, Page 16, Lines 7-8), Goldberg clearly fails to teach the Applicant's claim limitations.

With regard to Lehman, the Response to Arguments section seems to suggest that Lehman's bit string is a first state of a first logic circuit and that the individual bits of that bit string include logic circuits having their own first state. (Office Action, Page 22, Line 15 – Page 23, Line 4). In order to clarify the claim language, the Applicant has amended independent claim 10 to recite "wherein the first state of the first logic circuit is separate from the first state of the second logic circuit and the first state of the third logic circuit." Thus, Lehman's mere disclosure of a bit string clearly fails to teach the Applicant's claim limitations. Also, the Response to Arguments section alleges that the Applicant's claims do not distinguish from looking at an entire bit string as taught by Lehman. However, as shown above, Lehman's mere disclosure of "0" bits in a bit string fails to remedy the deficiencies of Goldberg in that the combination of references clearly fail to teach "wherein **the first state of the first logic circuit comprises a number of available memory segments** in the first memory block, **said number of available memory segments corresponding to at least the first state of the second logic circuit and the first state of the third logic circuit**," and "wherein the **first state of the first logic circuit** is **separate from** the **first state of the second logic circuit and the first state of the third logic circuit**," as recited in Applicant's independent claim 10. Because the combination of Goldberg in view of Lehman fails to teach or suggest all the claim limitations, a rejection under 35 U.S.C. §103(a) cannot be maintained.

Regarding claim 13, Applicant respectfully submits that the proposed combination of references fails to teach, suggest, or disclose at least, for example, "wherein the second state of the first logic circuit comprises an offset to available memory," as set forth in Applicant's independent claim 13.

The Response to Arguments section of the Office Action alleges that "the pending claims do not require the second state of the first logic circuit to point to an absolute address, but merely to comprise information indicating an offset to available memory." (Office Action, Page 24, Lines 12-14). The Applicant notes that "information indicating an offset to available memory" is different than an offset to a starting point for a search for available memory as disclosed by Lehman. Regardless, the Applicant has amended independent claim 13 to clarify that **the offset is to available memory, not merely a hint or starting point to look for available memory**. As stated in Lehman and acknowledged by the Office Action, Lehman merely discloses "['pointer array 124 permit the data manager to determine immediately if it should look in a given allocation page for a given buddy segment size and **provide a place to start looking for a segment** of a particular size' (Co. 9, lines 53-60) wherein 'the pointer array 124 **might** point to a buddy segment that is available...but on other occasions **the pointer array might point to a segment that was recently allocated**.... Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least **a correct starting point for a search** for that size buddy segment' (Col. 10, lines 1-10) (Figure 7 and related text)]." (Office Action, Page 24, Lines 3-17 (emphasis added)). Further, the Applicant appreciates the Examiner's recognition that Goldberg "doesn't expressly disclose the second state of the first logic circuit comprise information indicating an offset to available memory." (Office Action, Page 18, Lines 19-20). Therefore, the combination of Goldberg and Lehman cannot disclose "wherein the second state of the first logic circuit comprises an **offset to available memory**." Because the combination of Goldberg in view of Lehman fails to teach or suggest all the claim limitations, a rejection under 35 U.S.C. §103(a) cannot be maintained.

The Applicant further notes, as discussed in more detail below, that there is no motivation to combine Goldberg and Lehman because Goldberg explicitly criticizes and discredits the considerable waste of storage space and prohibitive sizes of multiple buffer pool implementations as taught by Lehman. One skilled in the art, upon reading Goldberg, would clearly be discouraged from using multiple buffer pools to optimize memory allocation as taught by Lehman. Thus, despite Lehman's efforts to make multiple buffer pool implementations require less space to store allocation information, one of ordinary skill in the art would not have found that the combined teachings of Goldberg and Lehman suggest Applicant's claim limitations because Goldberg teaches staying away from multiple buffer pool implementations altogether. Further, the combination of the references would be inoperable together. Because the combined teaching of Goldberg and Lehman would not have been construed by one of ordinary skill in the art as suggesting the limitations of Applicant's claims, the rejections under 35 U.S.C. §103(a) cannot be maintained.

The Applicant respectfully submits that, based upon the above, the proposed combination of Goldberg in view of Lehman fails to teach or suggest by themselves or in combination all of the limitations of Applicant's independent claims 10, 13 and 26, and that the rejections of claims 10, 13 and 26 under 35 U.S.C. §103(a) cannot be maintained. Therefore, Applicant respectfully requests that the rejections of claims 10, 13 and 26 under 35 U.S.C. §103(a), be withdrawn.

Because dependent claims 12, 14-15 and 27 depend, directly or indirectly, from independent claims 10, 13 or 26, and because claims 10, 13 and 26 are allowable over the proposed combination of references, the Applicant asserts that claims 12, 14-15 and 27 are also allowable over the proposed combination of references and that the rejections of dependent claims 12, 14-15 and 27 are now moot. The Applicant further submits that each of claims 12, 14-15 and 27 is independently allowable. Thus, the Applicant respectfully requests that the rejections of claims 10, 12, 13-15 and 26-27 under 35 U.S.C. §103(a), be withdrawn.

Rejections Under 35 U.S.C. §103(a) – Goldberg, Lehman and Rozario (Claims 1-9 and 25)

In points 11-20 on pages 6-13 of the Office Action, independent claim 1 and dependent claims 2-9 and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over Goldberg (U.S. Patent No. 6,874,062) in view of Lehman (U.S. Patent No. 6,658,437) and further in view of Rozario et al. (U.S. Publication No. 2004/0078525, hereinafter "Rozario"). The Applicant respectfully traverses the above-mentioned rejections for at least the following reasons.

Regarding claim 1, the Applicant respectfully submits that there is no motivation to combine Lehman or Rozario with Goldberg because Goldberg explicitly criticizes and discredits the considerable waste of storage space and prohibitive sizes of multiple buffer pool implementations as taught by Lehman and linked list implementations as taught by Rozario. The Applicant notes that a disclosure that criticizes, discredits, or otherwise discourages the solution claimed of a second disclosure, teaches away from the combination of disclosures. *In re Fulton*, 391, F.3d 1195, 1201 (Fed. Cir. 2004). Goldberg unequivocally criticizes, discredits and otherwise discourages optimizing memory allocation using multiple buffer pools as taught by Lehman or linked lists as taught by Rozario. For example, Goldberg explicitly states that the use of multiple buffer pools as taught by Lehman "results in a considerable waste of storage space." (Goldberg, Column 2, Lines 34-35). As another example, Goldberg explicitly criticizes the amount of storage space consumed by data structures such as linked lists. (Goldberg, Column 2, Lines 35-44). Instead of multiple buffer pools and linked lists, Goldberg teaches a hierarchical bitmap structure noting that such bitmaps only require a single bit "to describe whether each section of storage is allocated, a much smaller amount of memory is associated with the use of bitmaps as compared to the use of linked lists." (Goldberg, Column 3, Lines 5-9).

One skilled in the art, upon reading Goldberg, would clearly be discouraged from using multiple buffer pools and/or linked lists to optimize memory allocation as taught by Lehman and Rozario. Thus, despite Lehman's efforts to make multiple buffer pool implementations require less space to store allocation information, one of ordinary skill in the art would not have found that the combined teachings of Goldberg and Lehman suggest Applicant's claim limitations because Goldberg teaches staying away from multiple buffer pool implementations altogether.

Additionally, the Office Action alleges that the motivation to combine Rozario's free list 502 with the teachings of Goldberg and Lehman is "to provide higher speed and efficiency in memory accesses (Refer to Rozario, pars. 0005, 0051 and 0056)." (Office Action, Point 12, Pages 9-10). However, it is not Rozario's free list 502 in memory bank 410 that increases speed and efficiency in memory accesses as alleged in the Office Action. Rather, as explicitly stated in the sections of Rozario cited in the Office Action, Rozario teaches that its stack-based caching scheme is what reduces the memory bank 410 accesses. (Rozario, Paragraphs [0005], [0051] and 0056]). In other words, the use of Rozario's free list 502 of memory bank 410 does not provide higher speed and efficiency in memory accesses as alleged by the Office Action. Additionally, the Applicant notes that speed and efficiency are not problems in Goldberg. Instead, Goldberg solves the problem of wasted storage space by systems that use linked lists (like Rozario) by avoiding the use of linked lists altogether. (*See e.g.*, Goldberg, Column 1, Line 51 – Column 2, Line 56, and Column 3, Lines 5-9 and 22-29).

Put simply, Goldberg could not be clearer in its criticism of multiple buffer pools and linked lists. Further, the combination of the references would be inoperable together. Because the combined teaching of Goldberg, Lehman and Rozario would not have been construed by one of ordinary skill in the art as suggesting the limitations of Applicant's claims, the rejection under 35 U.S.C. §103(a) cannot be maintained.

The Applicant respectfully submits that, based upon the above, one of ordinary skill in the art would not have combined Goldberg in view of Lehman and further view of Rozario and that such combination would be inoperable. Therefore, Applicant respectfully requests that the rejections of claim 1 under 35 U.S.C. §103(a), be withdrawn.

Because dependent claims 2-9 depend, directly or indirectly, from independent claim 1, and because claim 1 is allowable over the proposed combination of references, the Applicant asserts that claims 2-9 are also allowable over the proposed combination of references and that the rejections of dependent claims 2-9 are now moot. The Applicant further submits that each of claims 2-9 is independently allowable. Thus, the Applicant respectfully requests that the rejections of claims 1-9 and canceled claim 25 under 35 U.S.C. §103(a), be withdrawn.

Rejections Under 35 U.S.C. §102(b) and 103(a) – Goldberg, Lehman and Rozario (Claims 24-27)

In points 8-9 on pages 4-5 of the Office Action, claim 24 was rejected under 35 U.S.C. §102(b) as being anticipated by Goldberg. In points 12, 22 and 24 on pages 6-10 and 14-19, claims 25-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Goldberg and Lehman, or Goldberg, Lehman and Rozario. The Applicant respectfully traverses the above-mentioned rejections for at least the following reasons.

Regarding claims 24-25, the Applicant notes that independent claim 24 has been amended to incorporate the limitations of dependent claim 25, which is currently canceled. For reasons generally analogous to those stated previously with regard to claim 1, the Applicant submits that claim 24 is allowable over Goldberg, and over Goldberg in view of Lehman and further in view of Rozario.

Regarding claim 26, the Applicant notes that claim 26 has been rewritten in independent form including all the limitations of previous independent claim 24. For reasons generally analogous to those stated previously with regard to claim 10, the Applicant submits that claim 26 is allowable over Goldberg, and over Goldberg in view of Lehman and further in view of Rozario.

Further, the Applicant notes that claim 27 depends from independent claim 26. Thus, for reasons generally analogous to those stated previously with regard to claim 26, the Applicant submits that claim 27 is allowable over Goldberg, and over Goldberg in view of Lehman and further in view of Rozario. The Applicant also submits that Applicant's dependent claim 27 is independently allowable for reasons generally analogous to those stated previously with regard to claim 13.

Final Matters

The Office Action makes various statements regarding former claims 1-10, 12-15 and 24-27, 35 U.S.C. § 102(b), 35 U.S.C. § 103(a), the Goldberg reference, the Lehman reference, the Rozario reference, one of ordinary skill in the art, etc. that are now moot in view of the above-mentioned amendments and/or arguments. Thus, the Applicants will not address all of such statements at the present time. However, the Applicants expressly reserve the right to challenge such statements in the future should the need arise (e.g., if such statements should become relevant by appearing in a rejection of any current or future claim).

Applicant reserves the right to argue additional reasons supporting the allowability of claims 1-10, 12-15, 24 and 26-27 should the need arise in the future.

CONCLUSION

Applicant respectfully submits that claims 1-10, 12-15, 24 and 26-27 are in condition for allowance, and requests that the application be passed to issue.

Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Date: March 5, 2010

Respectfully submitted,

/Philip Henry Sheridan/
Philip Henry Sheridan
Reg. No. 59,918
Attorney for Applicant

McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
(T) 312 775 8000
(F) 312 775 8100